Correlating SEM and SPM for Nanoprobing in Failure Analysis

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***Abstract*-A compact nanoprober suitable for SEM/FIB is presented. Each of the eight probes can be biased and scanned over the sample surface, allowing for the acquisition of current flow images (CI) with sub-pA resolution. The correlation of SEM and CI is used to locate leakages in 22 nm SRAM devices.**

I. INTRODUCTION

Within the last decades, the feature widths of semiconductor devices have become too small to be resolved by state-of the art optical microscopes, and other imaging techniques such as Scanning Electron Microscopes (SEM) or Scanning Probe Microscopes (SPM) have become indispensable. For some analyses of device failures a combination of imaging and electrical measurements is required [1]. Nowadays, one can find nanoprobers that are either based on SPM [2] or SEM [3] imaging techniques. For the SPM based nanoprobers, each probe consists of an Atomic Force Microscope (AFM) equipped with a conductive tip. For the SEM based systems, nanopositioners without force feedback are placed within a SEM.

Both approaches described above have advantages and disadvantages. Landing probes on a desired device is much easier for the SEM prober, as the SEM image gives immediate visual feedback. In contrast, the AFM prober requires many subsequent AFM images by each probe in order to align the probes with respect to each other and with respect to the device, which can be very time consuming. One advantage of the conductive AFM probing is the combination of topography images with electrical transport properties. This allows easy identification of leakages or shorts on the chip.

II. EXPERIMENTAL SETUP

In this work we present a very compact nanoprober that combines the advantages of SEM and SPM nanoprobers in one system.

The setup consists of a nanoprober (Kleindiek Prober Shuttle PS8) with 8 probes and an xyz substage (see Figure 1) mounted on the stage of an SEM (Zeiss Supra 40). An interface for positioning the probes and the sample with nanometer precision as well as the controls for all electrical measurements are provided by a software suite (Advanced Probing Tools (APT)).

Besides the complete measurement recipes for electrical characterization of semiconductor devices with stationary probes landed on the device, the APT suite offers the possibility for SPM based electrical measurements. In this so-called constant height STM mode, a voltage biased probe is scanned at "constant height" over the sample surface. The resulting current flow to a second probe or to the bulk contact can be simultaneously monitored with sub-pA resolution. A typical current image can be acquired in a few seconds in a scan range of up to 1.5 µm x 1.5 µm [4].

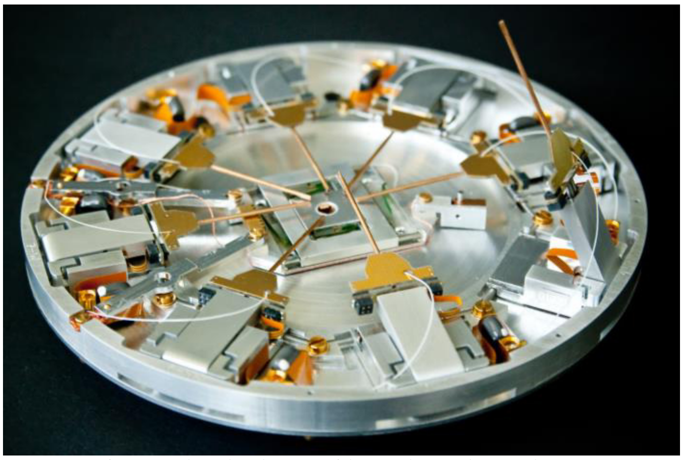

Fig. 1. Prober shuttle PS8 with 8 probes and xyz substage (14 cm diameter, 1 cm height)

Each probe (or the substage) can be selected as the "scanning" voltage source or the "stationary" current sink, which allows for a very flexible definition of the expected current path enabling a powerful method for the visualization of faults in the integrated circuits (IC).

III. RESULTS

In this section, some exemplary nanoprobing results together with current flow images obtained on a commercially available IC manufactured with 22 nm technology are demonstrated. The sample was prepared by chemical mechanical polishing down to the metal1 and contact layer.

A. Nanoprobing

With the help of the SEM image, probe needles with tip radii down to 5 nm can be safely landed on contact pads in the region of interest. Physically landing probes does not ensure good electrical contact to the contact pads, thus the contact resistance of each probe needs to be optimized. In case of a device under test (DUT) with several contact pads, it is hard to know which of the probes' electrical contact needs to be optimized. The APT software provides a quick and efficient way to identify each

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probes' contact to the DUT. With the Live Contact Tester (LCT), a series of current voltage curves (IVCs) is measured for each probe with a repetition rate of 10 Hz. This real-time display of each probe's signal allow a differentiation of the contacts the probes are connected to, e.g. a diode connection to bulk, or a resistance to a second prober. Probes connected to each other or to the bulk via the DUT show distinctive IVCs, such as an ohmic or a diode behavior.

While the LCT measurement is active, each probe can be re-positioned (without the use of the electron beam, thus minimizing e-beam induced contamination) in order to minimize the probe’s contact resistance. In the case of a transistor's gate contact, this method may not work, since some gate contacts do not have a connection to the bulk or to any other of the transistor's pads. In order to optimize the gate contact, the APT software provides a module for acquiring a set of source-drain curves at a high rate of repetition. The electrical contact to the transistor's gate can be optimized by re-positioning the corresponding tip until the transistor's source-drain current is maximized. Finally, the transistor's IVC can be measured by a (remotely controlled) Keithley 4200 parameter analyzer.

Figure 2 shows a nanoprobing example: A contacted n-MOS transistor on a 22 nm SRAM device. The different IVCs recorded with the Keithley 4200 correspond to different gate voltages. The SEM image illustrates the connection assignments for the contacted transistor.

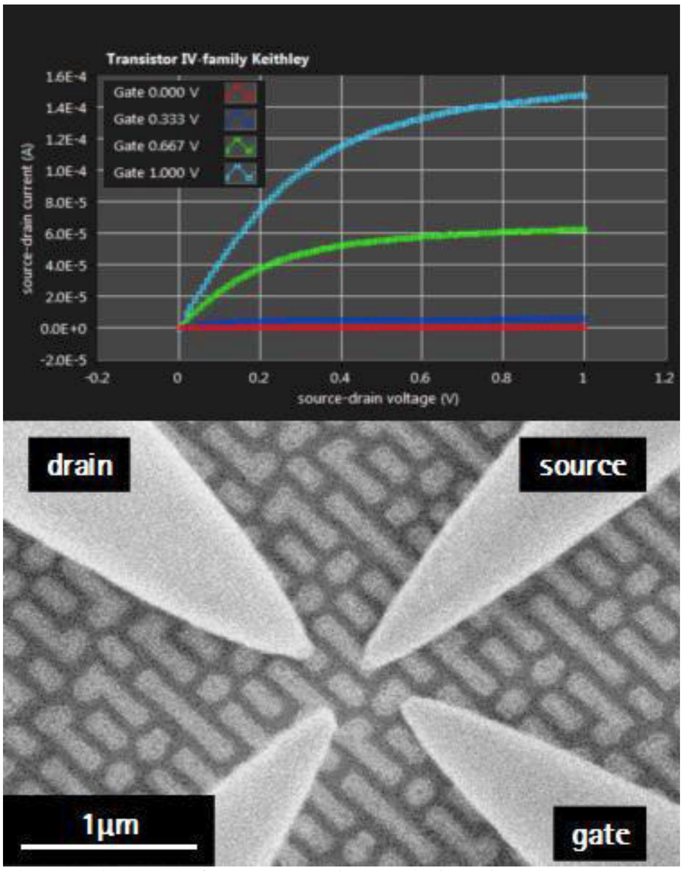

Fig. 2. Typical IVCs of a n-MOS transistor on the investigated 22 nm IC (top). SEM image of corresponding transistor with the connection scheme (bottom).

B. Current Imaging

For the detection of an electrical fault in an IC, nanoprobing in a suspicious region of interest can be time consuming. Current Imaging offers a fast and efficient way to scan probe tips or the substage in an area of up to 1.5 µm x 1.5 µm [4] and to acquire an image of the local current flow in order to identify and localize the faulty contact. The scan area of a few square microns seems to be complementary to the spatial resolution of other (optical) defect localization methods such as the optical beam induced resistance change (OBIRCH) method. Combining SEM imagery (the probes can be observed while the scan takes place) and the resulting current images enables correlative microscopy.

Figure 3 shows an overlay of the SEM image with (semi-transparent) current images on the 22 nm chip. The SEM image was inverted for a better illustration of the match between the SEM and CI image. In this case, a voltage of V_{out}= +1 V or -1V was applied to the probe tip on the right side. The current flow was measured with the stationary probe tip, landed on a contact pad to the left of the scan region. The current flow is measured while scanning the sourcing probe in contact-mode above the sample surface. Depending on the polarity (+ or - 1 V) of the biased tip, n-MOS or p-MOS contacts become visible in the current image.

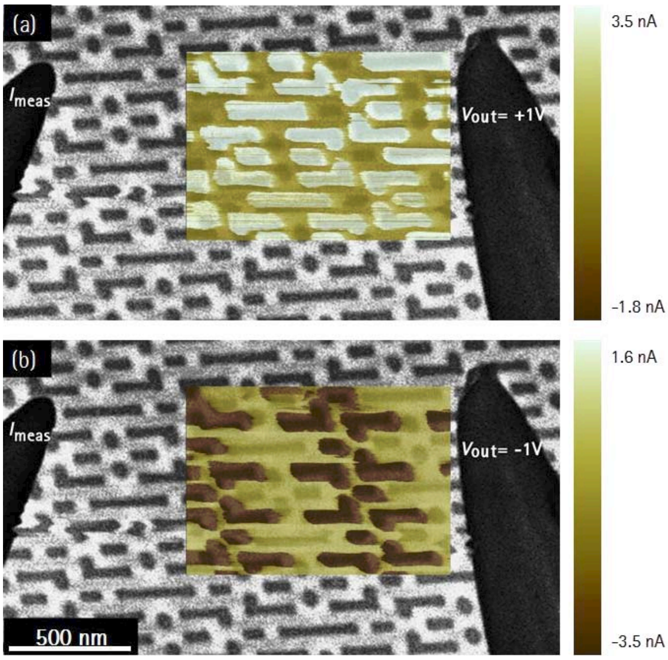

Fig. 3. Overlay of an SEM image with a current image on a 22 nm chip. The scanning probe (right) was biased at a voltage of (a) Vout=1 V and (b) Vout=-1 V. The stationary probe (left) was used as a current sink to measure the current flow between the two probes.

Not only the polarity of the biased tip's voltage but also the definition of the current path have a strong impact on the obtained current image. The APT software suite's CI module allows for an arbitrary definition of the current flow path. A signal switching unit enables routing any probe tip to the current sink and any other tip or the substage to the current source.

A current image obtained with a sourcing substage and a sinking probe tip is shown in Figure 4 (a). The voltage applied at the scanning substage was V = -0.6 V. The current image reveals a homogeneous current flow over the entire scan area, i.e. the same kind of contact pads have identical color (current). However, a variation of current flow can be observed among different contact pads, e.g. the L-shaped pads have higher current flow than the long bars. The circular gate contacts (c.f. SEM images in Figure 3) are not visible in the current image.

In Figure 4 (b), the current image is qualitatively different. Here, the current was sinked by the bulk and by a second stationary tip in contact with a pad outside the scanned area (close to the top right position of the scan area). The current was measured by the stationary tip only. The voltage at the scanning tip was kept at V= -0.52 V. In this situation only the contact pads corresponding to the source and sink of the same well yield a strong signal. In addition one can observe a current flow gradient from top to bottom, which is due to the larger distance and thus higher resistance between source and sink contact pads at the bottom of the scan area. The contact pads of nearby wells are also slightly visible in the current image however they show about one order of magnitude less current flow.

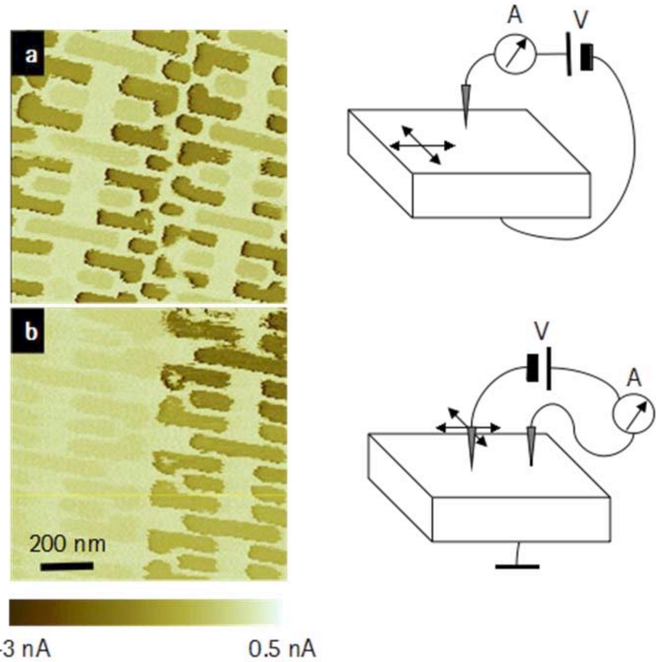

Fig. 4. Current flow image with different flow path definitions:
a) Current source via bulk signal (V=-0.6V), substage is scanning while stationary probe tip measures current. Current image shows homogeneous current flow over the chip.
b) Current source at scanning probe (V=-0.52V), bulk and second stationary probe landed on a contact pad acts as sink. The current is only measured at the second tip. Only the contact pads of the same well appear as strong signal in the current image.

Figure 5 shows an overlay of an SEM image with a current image. In the full scan image (top) one out of 16 circular gate contacts was slightly visible in the scan. A zoomed scan of the area clearly resolved this gate contact's leakage. The identification of the gate contact in the SEM image can be performed by simply moving the tip to the faulty gate contact within the CI module's GUI. In the SEM image the probe needle would then point to the defect position.

The investigation of the physical origin of the gate leakage is beyond the scope of this paper. However, if the current imaging was performed inside a FIB/SEM, it would be straightforward to further de-process the sample in-situ, e.g. to prepare a TEM lamella.

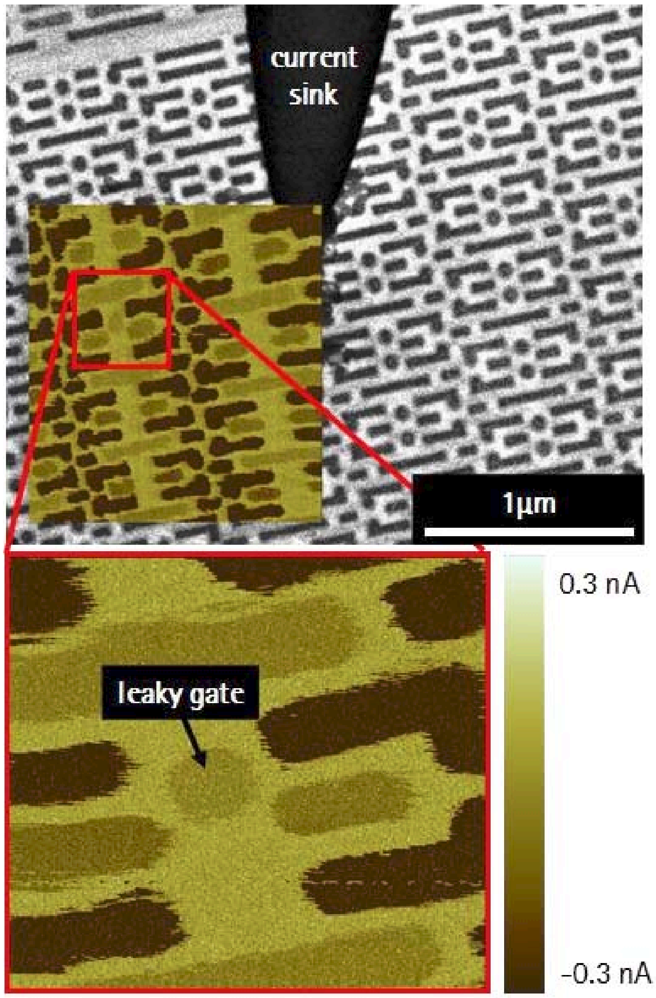

Fig. 5. Overlay of an SEM image with a current image of a 22 nm IC. The scanning substage was biased at a voltage of V=-0.6 V. The current flow was measured at a stationary probe tip (labeled current sink). Zoomed area shows a leaky circular gate contact.

IV. Summary

In this paper, case studies on a commercially available 22 nm IC are presented in order to describe the powerful method of the combined SEM and SPM nanoprober. Correlation of the SEM image with the CI image can reveal the origin of the defect or at least allow for a localization of the defect. If the experiment is performed inside a FIB/SEM tool, further de-processing of the sample in-situ is possible yielding fast and efficient failure analysis.

Acknowledgment

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[4] As the scanning is performed only in "fine mode", the scan range and the pixel resolution of a CI image is limited by the Piezo range of the scanning tip or substage. For the PS8 by default the scan range is 1.5 µm x 1.5 µm. With an (optional) different scanner higher scan ranges are feasible.